ELSEVIER

Available online at www.sciencedirect.com
SCIENCE DIRECT®

Nuclear Instruments and Methods in Physics Research A 511 (2003) 64–67

NUCLEAR INSTRUMENTS & METHODS IN PHYSICS RESEARCH
Section A

www.elsevier.com/locate/nima

CMS pixel detector—overview ☆

L. Cremaldi

Department of Physics and Astronomy, University of Mississippi, University, MS 38677, USA

For the CMS Collaboration

Abstract

Pixel detectors are being built for use at the Large Hadron Collider beginning in the year 2007. We present an overview of the Compact Muon Solenoid Pixel Detector effort.
© 2003 Elsevier B.V. All rights reserved.

PACS: 13.20.Fc; 13.30.Ce; 14.40.Lb

Keywords: Pixel detector; Vertex detector

1. Introduction

A Silicon Pixel Detector will be installed at the Large Hadron Colliders (LHCs) Compact Muon Solenoid (CMS) experiment [1]. It covers an η range $-2.5 \leqslant \eta \leqslant 2.5$ matching the acceptance of the central tracker. The pixel detector's $150 \times 100\ \mu m$ cells provide high-resolution 3D space points required for charged track pattern recognition. With position resolution of approximately $15\ \mu m$ in both coordinates it can determine the impact parameter of charged particles with high precision. This feature will allow for the reconstruction of secondary vertices from b and τ decays (jets), and formation of seed tracks for the outer track reconstruction and L2/L3 triggering [2].

The pixel detector, Fig. 1, consists of three barrel layers with two end-cap disks on each side. The three barrel layers will be located at mean radii of 4.4, 7.3 and 10.2 cm, respectively, and will be 53 cm long. The two end disks, extending from 6 to 15 cm in radius, will be placed on each side at $z = \pm 34.5$ and ± 46.5 cm. The forward detectors are tilted at 20° in a turbine-like geometry to induce charge sharing.

The inner pixel layers will be exposed to radiation fluence as high as $5 \times 10^{14}\ cm^{-2}\ s^{-1}$ equivalent to 1 MeV neutron flux, requiring a detector and electronics of radiation-hard design.

Each pixel detector readout unit consists of a 53×52 silicon diode array which is bump bonded to a matching readout chip. The bonding pad on the readout side is connected to an analogue low-noise pre-amp and a digital readout block both in close proximity. On the periphery of the readout chip are the data lines, control logic, buffers, and bias voltage. The readout chip contains about

☆Presented at VERTEX 2002 (Kona Hawaii, November 2002, representing the CMS Collaboration).

E-mail address: cremaldi@phy.olemiss.edu (L. Cremaldi).

0168-9002/03/$ - see front matter © 2003 Elsevier B.V. All rights reserved.
doi:10.1016/S0168-9002(03)01752-2

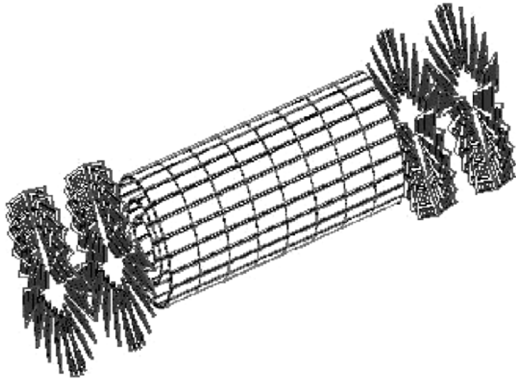

Fig. 1. CMS pixel detector, three barrel and two forward disks shown.

400,000 transistors. The total channel count for these detectors is large, with approximately 50 million pixels in the final configuration. A formidable challenge lies ahead in areas of (1) design of a radiation hard readout chip and supporting electronics, (2) radiation hard sensor design and layout, (3) signal and bias interconnects and busing, (4) mechanical support and cooling, and (5) overall performance.

2. Readout chip and token bit manager

The 53×52 pixel readout chip is laid out in a 26 double column configuration. A token bit manager chip (TBM) [3] controls the readout scan (40 MHz) of a group of readout chips. Both the readout chip and TBM are being designed in $\frac{1}{4}$ μm bulk CMOS technology, providing the most rad-hard solution. The total equivalent noise charge of the analogue front end remains $\leqslant 500$ electrons, projecting to years of LHC running. The chip will operate with a pixel threshold of about 2500 electrons. The readout chip generates about 90 μW per pixel of heat load.

A token scan, initiated by the TBM, performs a double-column readout of hit pixels storing charge above the threshold. A common pixel chip threshold is set by a DAC register. Each pixel front end contains a 4(or 5)-bit DAC trim for individual threshold adjustment. Any signal data over threshold are transferred to the periphery in less than eight bunch crossings, 200 ns, and is stored in a 24 deep buffer. In this time there is typically $\leqslant 10^{-3}$ chance of a second hit. Upon receiving a trigger decision, with 3.2 μs latency, the analogue hit information are read out through an optical link.

Heavily ionizing radiation deposits on the electronic digital and analogue sections can cause event upsets and readout latch-ups, both affecting data levels, data flow, and control. Estimates are as high as 10^{-6} upset per bits near the inner pixel tracker. Constant refreshing of threshold DACs and system resets will be needed for a safe and reliable operation.

3. Silicon diode sensor

The harsh radiation environment within tens of centimeters of the interaction region will quickly degrade the performance and lifetime of the silicon sensor. Silicon sensors of n+ implants on n-bulk and a metallized p-backside are being used. After a dose of order 10^{12} cm^{-2} the n-bulk will type-invert forming an effective p-bulk substrate. The diode is now n+ pixel implant on p-substrate.

On the n-side of the wafer the charge collecting pixels are defined by n-implants surrounded by isolating p-stop rings. The design of these p-stops are critical in providing pixel-to-pixel isolation and preventing leakage currents. A further charging problem may develop if a pixel is not well-connected to its readout amplifier. The p-stop design must compensate and dissipate any build up of charge.

The p-backside of the wafer requires metallization for biasing. Here the sensor is biased by typically 300–500 V, and care must be taken in isolating the biased metallization edge from the bonded readout chip. A series of guard rings placed near the p-side edge carefully lowers the bias voltage to ground to avoid possible corona or breakdown.

We presently believe that oxygenated n-type silicon provides the most rad-hard bulk material for sensor production. Studies of the radiation hardness properties of silicon are ongoing [4].

4. Bump bonding and interconnects

The sensors are diced into 2×8 sensor arrays for the barrel and various sizes for the forward disks. The readout chips are bump bonded to the sensor arrays. The bumps are approximately 25 μm of indium or Pb-Sn solder, which is still under investigation. Two methods of bonding are under consideration. In indium bonding the readout chip and sensor surfaces are prepared for metal evaporation. The sensor and readout chip are then carefully aligned in a flip-chip bonder and then mechanically pressed to form the bond. This process results in a low bond failure rates ($\leqslant 10^{-3}$). Also a reflow technique is being investigated. The pads are prepared for soldering in an under-bump metallization stage, then the solder is electroplated on. The chips are aligned and reheated (180°C). The technique is self-aligning to a great degree, because of reflow bonding forces. This technique results in the high strength and very reliable bonds common to the chip packaging industry. Combinations of bump bonding and reflow are also being considered.

The sensor arrays are attached to a hybrid circuit for placement on the detector. The p-side of the readout unit is glued to a very high density interconnect (VHDI), multilayer copper-on-Kapton flex mounted onto a Si substrate with a matching CTE epoxy. A number of wire bonds must be made to the sensor and the readout chip providing bias and signal connections. The VHDI is then mounted to a copper-on-Kapton flex HDI of less complexity and additional wire bonds are made. This two-phase strategy is seen to pay off in the checking and debugging of the individual detector pieces during fabrication steps and then onto the final detector.

5. Material budget, cooling, and services

The total material budget of the Si-pixel system can be costly due to the high density of components, busing, and chip stacking. The readout chip, sensor, and Si substrate, each ≈ 300 μm thick, amount to nearly a mm of Si. Adding in the VHDI/HDI Kapton flex we come to a fractional radiation length $X/X_0 = 0.025$ per tracking layer.

An additional material budget is imposed by the support structure and cooling. At 90 μW per pixel a few tens of kW of power must be removed from the detectors. Presently conventional liquid fluorocarbon coolant is used [5]. Estimates of the contributions from support and cooling structures is $X/X_0 = 0.020$ raising the total material budget to $X/X_0 \approx 0.045$ per tracking layer at normal incidence.

The annual removal and reinsertion of the pixel detector for beam pipe bakeout purposes requires that the pixel detectors be inserted into final position on service tubes. The barrel and forward detectors tubes are split into halves for insertion along rails. The rails are mounted above and below the beam pipe. All cooling and electrical services are brought in along the service tubes. This modular and removable system will allow for easier service and repair.

6. Performance issues

Beam tests [6] and simulations of pixel performance are ongoing [7]. They show that the CMS pixels do achieve (10–20) μm hit resolution when fully depleted and that neighboring cells achieve considerable charge sharing due to $E \times B$ drift in the barrel and tilting in the forward disks.

A beam test of a current readout chip [8] design has been performed with a 350 Mev/c π-beam at PSI, delivering up to 30 MHz/cm^2 rate. Early results show a 5.5% inefficiency observed for beam telescope triggered events and a somewhat lower 3.5% inefficiency for superimposed calibration pulses. Although not operating at the full 40 MHz, this test is seen as a positive indication that the final bulk CMOS design will be totally functional at design specification.

7. Summary

We have made good progress in 2002 on the critical issues of readout chip and token bit manager design, bump bonding, and sensor

testing. The readout chip and token bit manager are being translated into $\frac{1}{4}$ μm technology. There are many details to be considered before installation in 2007.

References

[1] The CMS Tracker Technical Design Report, CMS/LHCC 98-6.
[2] T. Boccali, CMS Trigger, Nucl. Instr. and Meth. A, (2003) these proceedings, and CMS DAQ TDR, CMS/LHCC 2002-26.
[3] E. Bartz, The token bit manager chip for the CMS pixel readout, Contribution to Pixel 2002 Conference, Carmel, CA, USA, 9–12 September, 2002.
[4] D. Bortoletto, CMS FPIX sensor development, Nucl. Instr. and Meth. A, (2003) these proceedings.
[5] M. Atac, B. Gobbi, L. Cremaldi, J. Hoffman, Nucl. Instr. and Meth. A 476 (2002) 676.
[6] M. Atac, et al., Nucl. Instr. and Meth. A 488 (2002) 271.
[7] M. Swartz, CMS pixel simulations, Nucl. Instr. and Meth. A, (2003) these proceedings.
[8] W. Erdmann, The DMILL readout chip for the CMS pixel detector, Contribution to Pixel 2002 Conference, Carmel, CA, USA, September 9–12, 2002.